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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/615,567	07/08/2003	Dietrich Bonart	Z&P-INF-P10802	9016
24131	7590	08/04/2005	EXAMINER	
LERNER AND GREENBERG, PA P O BOX 2480 HOLLYWOOD, FL 33022-2480			WILCZEWSKI, MARY A	
			ART UNIT	PAPER NUMBER
			2822	

DATE MAILED: 08/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/615,567

Applicant(s)

BONART ET AL. 

Examiner

M. Wilczewski

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 23 May 2005.
- 2a) ☒ This action is **FINAL**.                      2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-21 is/are pending in the application.
- 4a) Of the above claim(s) 1-15 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 16, 17 and 19-21 is/are rejected.
- 7) ☒ Claim(s) 18 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 08 July 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All    b) ☐ Some \*    c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

### **DETAILED ACTION**

This Office action is in response to the remarks filed on May 23, 2005.

#### ***Election/Restrictions***

Applicant's election without traverse of the invention of group I, claims 16-21, in the reply filed on December 6, 2004, is acknowledged.

#### ***Priority***

Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

#### ***Drawings***

The Examiner approves the drawings filed on July 8, 2003.

#### ***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 16, 17, 19, 20, and 21 are again rejected under 35 U.S.C. 102(b) as being clearly anticipated by Dhong et al., U.S. Patent 4,954,854.

Dhong et al. disclose a vertical transistor which comprises at least one trench wall, see trench 20 in Fig. 5; a plurality of source and drain regions, reference numerals 18, 24, and 26 in Figs. 1 and 10; a channel region running essentially vertically on the trench wall between the source and drain regions; a gate electrode 32 shown in Fig. 12, a gate oxide 30 insulating the gate electrode 32 from the channel region, as shown in Fig. 12; and at least one insulating structure 16A for insulating between different vertical transistors, see Figs. 1 and 12 and column 5, lines 28-29. Note in Figs. 1 and 12 that insulation structure 16, 16A bounds gate electrode 32 at the uppermost portion of the trench. Since the gate electrode 32 is formed flush against insulation structure 16, 16A at the uppermost portion of the trench, as shown in Fig. 1, the gate electrode would have an internal angle  $\alpha$  of  $0^\circ$  with insulation structure 16, 16A. Also note that Dhong et al. teaches that the vertical transistor can be used in a DRAM cell, wherein the DRAM cell includes a capacitor and the vertical transistor formed above the capacitor, see Figs. 14 and 15.

#### ***Allowable Subject Matter***

Claim 18 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

### ***Response to Arguments***

Applicant's arguments filed May 23, 2005, have been fully considered but they are not persuasive. Applicants have argued that the reference numeral 32, which Dhong uses to indicate the gate electrode, imprecisely indicates the upper part of the trench. Applicants have further argued that upper part of the trench does not act as a gate, but, rather, acts as a connection between the word line and the gate. Accordingly, it is Applicants' position that the statement by the Examiner that "the gate electrode 32 is formed flush against insulation structure 16 at the uppermost portion of the trench", contradicts the definition of a gate. Therefore, it is Applicants' position that claim 16 is not anticipated by Dhong.

"Gate" is defined in the *Modern Dictionary of Electronics, Seventh Edition*, as one of the electrodes of a field-effect transistor. In *The Illustrated Dictionary of Electronics, Eighth Edition*, "gate" is defined as the input (control) electrode of a field-effect transistor. Dhong clearly teaches that the gate electrode is formed in the trench; see column 5, lines 62 and figure 1. Moreover, in column 6, lines 50+, Dhong teaches that the topography of the fabricated transistor is flat after gate level. Dhong clearly teaches that the gate of the field-effect transistor is formed in the trench. When a reference relied on either anticipates or makes obvious the claimed invention, the reference is presumed to be operable. In this case, since Dhong clearly discloses that the portion of polysilicon formed in the trench functions as the gate of the field-effect transistor, if, as Applicants have argued, the upper part of the polysilicon does not act as a gate, burden

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is on Applicants to provide **facts** rebutting the disclosure of Dhong. In addition, Applicants' arguments or those of Applicants' counsel cannot take the place of evidence in the record. *In re Schulze*, 145 USPQ 716, 718 (CCPA 1965); *In re Geisler*, 43 USPQ2d 1362 (Fed. Cir. 1997) ("An assertion of what seems to flow from common experience is just attorney argument and not the kind of factual evidence that is required to rebut a *prima facie* case of obviousness.") Factual evidence must be presented to support Applicants' argument that the upper portion of the polysilicon in the trench does not act as a gate, but, rather, acts as a connection between the word line and the gate.

In further response to Applicants' argument that the upper portion of polysilicon in the trench does not act as a gate, but, rather, acts as a connection between the word line and the gate, whether or not this portion of polysilicon functions as the gate seems irrelevant, since this upper portion is part of the gate. Arguably, the upper portion of the polysilicon in the trench is that portion **of the gate** that makes connection to the word line. Whether this portion of polysilicon acts as a gate or a connection to the word line, isn't this upper portion still a part of the gate?

***Conclusion***

**THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to M. Wilczewski whose telephone number is (571) 272-1849. The examiner can normally be reached on Monday and Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on 571-272-1852. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

A handwritten signature in black ink, appearing to be 'M. Wilczewski', with a stylized, flowing script.

M. Wilczewski  
Primary Examiner  
Tech Center 2800